IN THE DRAWINGS

Please approve the changes to Figs. 1, 2, 3, and 5 as indicated in red on the sheets attached to the accompanying Letter to the Official Draftsman.

IN THE CLAIMS

Please cancel claims 12, 15, and 23 without prejudice as to the subject matter underlying the claims.

Please amend claims 1, 3, 6, 7, 9, 11, 13, 14, 16-22, 24 and 25 as follows:

1. (Amended) A voltage doubler receiving at an input a continuous power voltage and supplying at an output a voltage having a value virtually double that of said continuous power voltage, the voltage doubler comprising:

a. an oscillator, powered by said continuous power voltage having a first output, and a second output in phase opposition to the first output,

b. a charge accumulation condenser having a first terminal connected to a potential reference and a second terminal connected to the output of the doubler,

c. a first charge transfer condenser having a first terminal connected to said first output of said oscillator, and

d. two inverters connected together in a loop [so as] to form a flip-flop having a first input connected to a second terminal of said first condenser, negative power terminals connected together to said continuous power voltage and

positive power terminals connected together to said second terminal of said charge accumulation condenser, and

e. a second charge transfer condenser having a first terminal connected to said second output of said oscillator and a second terminal connected to a second input of said inverters.

2. The voltage doubler in accordance with claim 1, wherein said inverters include MOS transistors which are virtually equal, and wherein corresponding bulk terminals of said MOS transistors are connected in such a manner as to create a one-way conduction path between said negative terminals and said positive terminals of said inverters.

3. (Amended) A voltage doubler receiving at an input a continuous power voltage and supplying at an output a voltage having a value virtually double that of said continuous power voltage, the voltage doubler comprising:

a. an oscillator powered by said continuous power voltage and having two outputs in phase opposition,

b. a charge accumulation condenser having a first terminal connected to a potential reference and a second terminal connected to the output of the doubler,

c. a first charge transfer condenser and a second charge transfer condenser having

first terminals respectively connected to the outputs of said oscillator,

d. a bridge comprising four diodes, having a positive terminal connected to the second terminal of said charge accumulation condenser, a negative terminal connected to said continuous power voltage and two [indifferent] intermediate terminals respectively connected to second terminals of said first charge transfer condenser and said second charge transfer condenser, and

e. four transistors having principal conduction paths connected in parallel with said four diodes and control terminals connected to the first charge transfer condenser and the second charge transfer condenser in such a way as to lower [the] a voltage drop along [the bridge] branches of the bridge when the doubler reaches a [at] steady state.

4. The voltage doubler in accordance with claim 3, wherein said four transistors are MOS type and are virtually equal.

5. The voltage doubler in accordance with claim 3, wherein said four diodes are respective bulk diodes of said four transistors.

6. (Amended) A voltage booster receiving at an input a continuous power voltage and supplying at an output a voltage higher than the continuous power voltage, the

voltage booster comprising:

a. an oscillator powered by said continuous power voltage, having two outputs in phase opposition,

b. a charge accumulation condenser having a first terminal connected to a first potential reference and a second terminal connected to the output of the booster, and

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator, and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation condenser and the input terminal connected to [a] the continuous power voltage,

wherein the at least one charging section comprises:

a first charge transfer condenser and a second charge transfer condenser having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two [indifferent] intermediate terminals connected to respective second terminals of said first charge transfer condenser and said second charge transfer condenser, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal ,

and wherein the value of the voltage of the output corresponds to said second potential

less the value of said first potential plus the product of said continuous power voltage and a number of the at least one charging section.

7. (Amended) The voltage booster in accordance with claim 6, wherein the switches of said bridge form two inverters connected together in a loop [so as] to form a flip-flop, having inputs connected to respective second terminals of said first charge transfer condenser and said second charge transfer condenser, negative power terminals connected together to said power input terminal and positive power terminals connected together to said charge output terminal.

~~8~~ 7. The voltage booster in accordance with claim ~~7~~ 6, wherein said switches include MOS transistors.

~~9~~ 8. (Amended) The voltage booster in accordance with claim ~~8~~ 7, wherein corresponding bulk terminals of said MOS transistors are connected in such a way as to create a one-way conduction path between said power input terminal and said charge output terminal when the switches are not conducting.

~~10~~ 9. The voltage booster in accordance with claim ~~7~~ 6, wherein said inverters are virtually equal.

10. (Amended) The voltage booster in accordance with claim 5, wherein said [first] power input terminal is connected to said continuous power voltage.

13. (Amended) An [electrically programmable and delectable] non-volatile memory device of [the] a type [powerable] powered with a low voltage comprising:

a. an oscillator powered by said [continuous power] low voltage, having two outputs in phase opposition,

b. a charge accumulation condenser having a first terminal connected to a first potential reference and a second terminal connected to [the] an output of the [booster] memory device, and

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation condenser and the input terminal connected to [a continuous power] the low voltage,

wherein the at least one charging section comprises:

a first charge transfer condenser and a second charge transfer condenser having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two [indifferent] intermediate terminals connected

to respective second terminals of said first charge transfer condenser and said second charge transfer condenser, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal,

and wherein the value of the voltage of the output corresponds to said second potential less the value of said first potential plus the product of said continuous power voltage and a number of the at least one charging section.

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14. (Amended) A voltage regulator having a low voltage drop between an input and an output of [the] a type having a MOS power transistor as an output regulation element and a voltage booster means having an output coupled to a control terminal of said power transistor to [hold said] maintain a conduction condition on the power transistor [in conduction condition with changes in the] when operating conditions of the regulator change, wherein the voltage booster means includes:

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a. an oscillator powered by [said] a continuous power voltage, having two outputs in phase opposition,

b. a charge accumulation condenser having a first terminal connected to a first potential reference and a second terminal connected to the output of the voltage booster means, and

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected

to the outputs of said oscillator and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation condenser and the input terminal connected to [a] the continuous power voltage,

wherein the at least one charging section comprises:

a first charge transfer condenser and a second charge transfer condenser having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two [indifferent] intermediate terminals connected to respective second terminals of said first charge transfer condenser and said second charge transfer condenser, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal ,

and wherein the value of the voltage of the output corresponds to said second potential less the value of said first potential plus the product of said continuous power voltage and a number of the at least one charging section.

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13 16. (Amended) The voltage multiplier of claim [15] 12, wherein the output means includes a charge accumulation condenser connected between the multiplied voltage and a potential reference.

14 17. The voltage multiplier of claim 13 16, wherein the output voltage is outputted at

the connection between the charge accumulation condenser and the multiplied voltage.

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~~18~~. (Amended) The voltage multiplier of claim [15] ~~14~~, wherein the oscillator is powered by the constant voltage.

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19. (Amended) A voltage multiplier receiving a constant voltage comprising:

an oscillator providing two outputs in phase opposition;

multiplying means connected to the constant voltage and the oscillator outputs for generating a multiplied voltage which is a multiple of the constant voltage; and

output means receiving the multiplied voltage for outputting a substantially constant output voltage which is a multiple of the constant voltage;

[The voltage multiplier of claim 15], wherein the multiplying means includes:

at least one first charge transfer condenser connected to one output of the oscillator;

at least one second charge transfer condenser connected to another output of the oscillator;

at least one bridge circuit having an input coupled to the constant voltage, an output providing the multiplied voltage, and at least two side inputs respectively coupled to the at least one first charge transfer condenser and the at least one second charge transfer condenser.

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~~20~~. (Amended) The voltage multiplier of claim ~~19~~, wherein:

the at least one first charge transfer condenser includes a plurality of first charge transfer condensers, each being connected to said one output of the oscillator;

the at least one second charge transfer condenser includes a plurality of second charge transfer condensers corresponding to the plurality of first charge transfer condensers, each of the second charge transfer condensers being connected to said another output of the oscillator;

the at least one bridge circuit includes a plurality of series connected bridge circuits corresponding to the plurality of first charge transfer condensers and plurality of second charge transfer condensers, each bridge circuit having two side inputs connected to a respective first charge transfer condenser and a respective second charge transfer condenser.

21. (Amended) The voltage multiplier of claim 19, wherein the at least one bridge circuit includes:

four diodes in a bridge arrangement such that a positive terminal is connected to the output , a negative terminal is connected to the input, and two [indifferent] intermediate terminals are connected to the side inputs; and

four transistors having principal conduction paths connected in parallel with the four diodes and control terminals connected to the side inputs.

22. (Amended) The voltage multiplier of claim 20, wherein each of the plurality of series connected bridge circuits includes:

four diodes in a bridge arrangement such that a positive terminal is connected to the output , a negative terminal is connected to the input, and two [indifferent] intermediate terminals are connected to the side inputs; and

four transistors having principal conduction paths connected in parallel with the four diodes and control terminals connected to the side inputs.

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24. (Amended) A method for generating a principal output voltage based upon a low constant input voltage comprising the steps of:

generating a first periodic signal;

generating a second periodic signal out of phase to said first periodic signal;

applying the first periodic signal to at least one first charge transfer condenser;

applying the second periodic signal to at least one second charge transfer condenser;

generating said output voltage based upon said input voltage, an output voltage of the at least one first charge transfer condenser, an output voltage of the at least one second charge transfer condenser;

[The method of claim 23,] wherein the step of generating the output voltage includes the steps of:

applying said input voltage, [an] the output voltage of the at least one first charge transfer condenser, [an] and the output voltage of the at least one second charge transfer condenser to inputs of a bridge circuit;

applying an output of the bridge circuit to a first terminal of a charge accumulation

condenser, a second terminal of the charge accumulation condenser being connected to a potential reference; and

providing said principal output voltage at said first terminal of the charge accumulation condenser.

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25. (Amended) A method for generating a principal output voltage based upon a low constant input voltage comprising the steps of:

generating a first periodic signal;

generating a second periodic signal out of phase to said first periodic signal;

applying the first periodic signal to at least one first charge transfer condenser;

applying the second periodic signal to at least one second charge transfer condenser;

generating said output voltage based upon said input voltage, an output voltage of the at least one first charge transfer condenser, an output voltage of the at least one second charge transfer condenser;

[The method of claim 23,] wherein:

the first periodic signal is applied to a plurality of first charge transfer condensers;

the second periodic signal is applied to a plurality of second charge transfer condensers; and

the generating step includes:

applying respective outputs of the plurality of first charge transfer condensers

and respective outputs of the plurality of second charge transfer condensers as inputs to a respective plurality of bridge circuits arranged in a series;

applying the input voltage to an input of a first bridge circuit in the series of the plurality of bridge circuits; and

providing an output of a last bridge circuit in the series of the plurality of bridge circuits as the output voltage.

REMARKS

In response to the Office Action mailed December 13, 1996, Applicant respectfully requests reconsideration. The drawings were objected to due to certain informalities. The specification was objected to under 35 U.S.C. § 112, first paragraph, as failing to provide an enabling disclosure. Claims 1-25 were rejected under 35 U.S.C. § 112, first paragraph, based upon the objection to the specification, and under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-25 were rejected under 35 U.S.C. § 103 as being unpatentable over Matsumura or Okada. The drawings and claims have been amended.

Proposed amendments to the drawings have been presented to correct the prior art labeling and the representation of P channel transistors. Applicants respectfully suggest that the specification is correct and provides an enabling disclosure. The polarities of the diodes shown in Figs. 3 and 5 are correct. As illustrated on the attached sheet, in an N channel transistor, the body and source are short-circuited together. This results in a bulk diode representation between